**AIC HW3**

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**Problem 1:**

|  |  |  |  |
| --- | --- | --- | --- |
|  | Acm (V/V) | Adm (V/V) | CMRR (V/V) |
| (a) | 165.6810m | -13.4153 | 79.7635 |
| (b) | 37.1281m | -4.0028 | 107.8105 |

**Problem 1 code:**

1. \*\*\*-----------------------\*\*\*

2. \*\*\*        setting        \*\*\*

3. \*\*\*-----------------------\*\*\*

4. .lib "~/U18\_HSPICE\_Model/mm180\_reg18\_v124.lib" tt

5. .TEMP 25

6. .op

7. \*\*\*-----------------------\*\*\*

8. \*\*\*       simulation      \*\*\*

9. \*\*\*-----------------------\*\*\*

10. .option post

11. .tran 0.1n 30u

12. .probe I(M1\_n)

13. .probe I(M2\_n)

14. .probe Vout=V(x,y)

15. \*.DC Vgs  0V 1.8V 0.05V sweep T 0 80 10

16.

17. \*\*\*-----------------------\*\*\*

18. \*\*\*      parameters       \*\*\*

19. \*\*\*-----------------------\*\*\*

20. .global VDD GND Vbs Vb

21.

22. \*\*\*-----------------------\*\*\*

23. \*\*\*       measure         \*\*\*

24. \*\*\*-----------------------\*\*\*

25. .meas tran Vx\_max  max  v(x)   from=0.1ns to=30us

26. .meas tran Vx\_min  min  v(x)   from=0.1ns to=30us

27. .meas tran Vx\_Vpp  param ='Vx\_max - Vx\_min'

28.

29. .meas tran Vy\_max  max  v(y)   from=0.1ns to=30us

30. .meas tran Vy\_min  min  v(y)   from=0.1ns to=30us

31. .meas tran Vy\_Vpp  param ='Vy\_max - Vy\_min'

32.

33. .meas tran Vin\_max  max  v(V\_diff+)   from=0.1ns to=30us

34. .meas tran Vin\_min  min  v(V\_diff+)   from=0.1ns to=30us

35. .meas tran Vin\_Vpp  param ='Vin\_max-Vin\_min'

36.

37. .meas tran Vout\_max  param ='Vx\_max - Vy\_min'

38. .meas tran Vout\_min  param ='Vx\_min - Vy\_min'

39. .meas tran Vout\_Vpp  param ='Vout\_max - Vout\_min'

40.

41. .meas tran Vdiff\_max  max  v(Vdiff)   from=0.1ns to=30us

42. .meas tran Vdiff\_min  min  v(Vdiff)   from=0.1ns to=30us

43. .meas tran Vdiff\_Vpp  param ='Vdiff\_max - Vdiff\_min'

44.

45. .meas tran Adm  param ='-Vout\_Vpp / Vdiff\_Vpp'

46. \*.meas tran Acm  param ='-Vx\_Vpp / Vin\_Vpp'

47. \*.meas tran CMRR  param ='Adm / Acm'

48.

49. \*MAX tells Hspice to take the max value of V/I of variable during t1 ~ t2

50. \*\*\*-----------------------\*\*\*

51. \*\*\*      power/input      \*\*\*

52. \*\*\*-----------------------\*\*\*

53. Vsupply VDD GND 3v

54. \*              SIN(Offset   Amplitude   Freq.   Delay )

55. V1      Vbs GND 0.6v

56. V2      Vb  GND 2v

57. Vcm     N0  GND 1v

58. V4      Vdiff  GND SIN(0   1m   100k  0)

59. EV+     V\_diff+ N0 Vdiff GND +0.5

60. EV-     V\_diff- N0 Vdiff GND -0.5

61. \*\*\*-----------------------\*\*\*

62. \*\*\*        circuit        \*\*\*

63. \*\*\*-----------------------\*\*\*

64. R1  VDD  X   5k

65. R2  VDD  Y   5k

66. M1\_n  X  V\_diff+    Virtual       GND    n\_18\_mm w=45u l=0.3u

67. M2\_n  Y  V\_diff-    Virtual       GND    n\_18\_mm w=45u l=0.3u

68. M5\_n  Virtual  Vbs        GND     GND    n\_18\_mm w=75u l=1u

69.

70. .subckt CKT\_A   Vin\_pos Vin\_neg  X   Y

71. R1  VDD  X   5k

72. R2  VDD  Y   5k

73. M1\_n  X  Vin\_pos    V       GND    n\_18\_mm w=45u l=0.3u

74. M2\_n  Y  Vin\_neg    V       GND    n\_18\_mm w=45u l=0.3u

75. M5\_n  V  Vbs        GND     GND    n\_18\_mm w=75u l=1u

76. .ends

77.

78. .subckt CKT\_B   Vin\_pos Vin\_neg  X   Y

79. M3\_p  X  X          VDD     VDD    p\_18\_mm w=10u l=0.3u

80. M4\_p  Y  Y          VDD     VDD    p\_18\_mm w=10u l=0.3u

81. M1\_n  X  Vin\_pos    V       GND    n\_18\_mm w=45u l=0.3u

82. M2\_n  Y  Vin\_neg    V       GND    n\_18\_mm w=45u l=0.3u

83. M5\_n  V  Vbs        GND     GND    n\_18\_mm w=75u l=1u

84. .ends

85.

86. .subckt CKT\_C   Vin\_pos Vin\_neg  X   Y

87. M3\_p  X  Vb         VDD     VDD    p\_18\_mm w=10u l=0.3u

88. M4\_p  Y  Vb         VDD     VDD    p\_18\_mm w=10u l=0.3u

89. M1\_n  X  Vin\_pos    V       GND    n\_18\_mm w=45u l=0.3u

90. M2\_n  Y  Vin\_neg    V       GND    n\_18\_mm w=45u l=0.3u

91. M5\_n  V  Vbs        GND     GND    n\_18\_mm w=75u l=1u

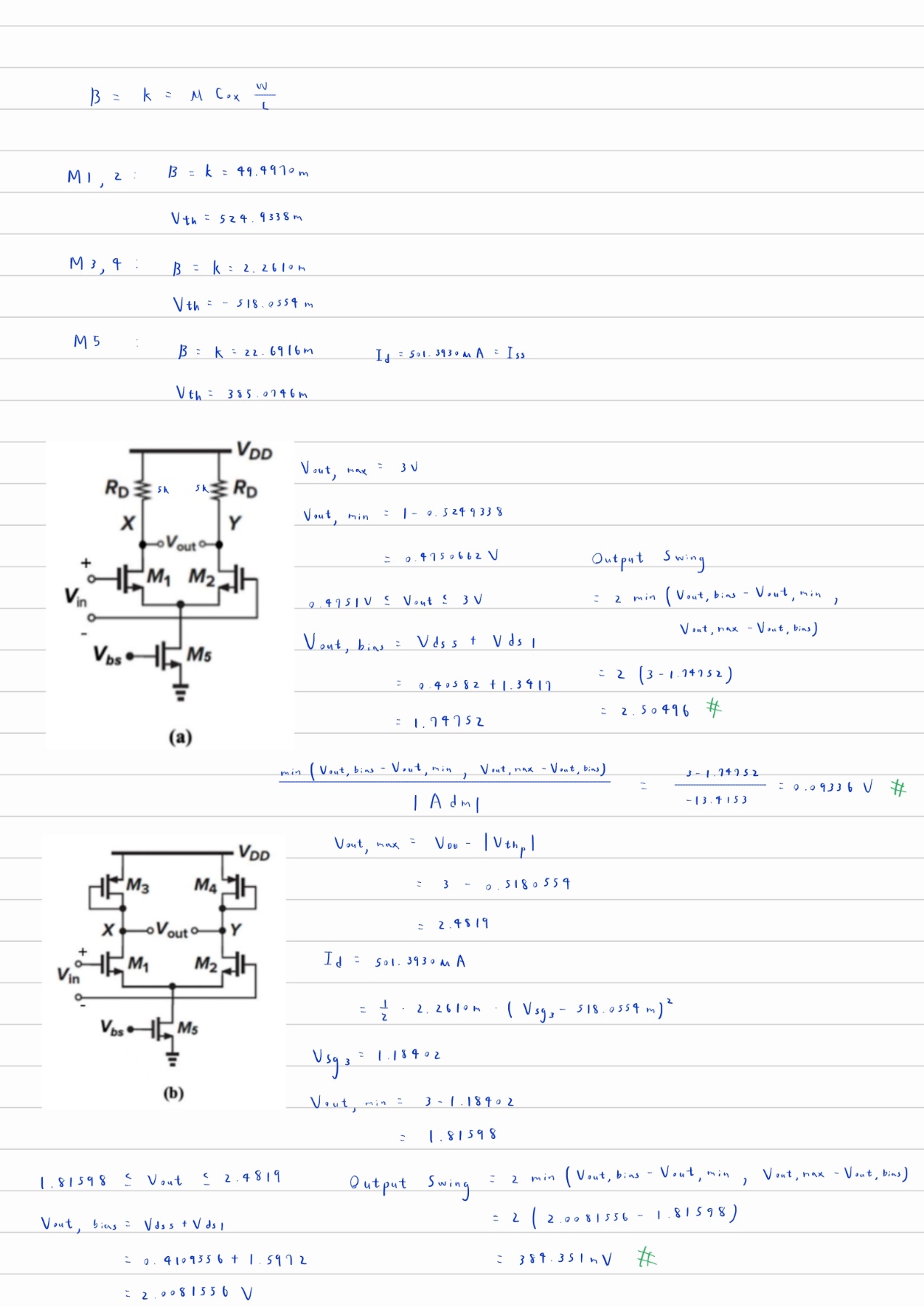
92. .ends

93.

94. .end

**Problem 2:**

**Derivation of Max Input Amplitude & Output Swing:**



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自動產生的描述

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | DC Gain (V/V) | Vout, bias (V) | Vout, min (V) | Vout, max (V) | Output Swing (V) | Max Input Signal Amplitude (V) |
| (a) | -13.4151 | 1.748 | 0.475 | 3 | 2.505 | 93.36m |
| (b) | -4.0028 | 2.008 | 1.816 | 2.482 | 384.351m | 48.01m |
| (c) | -30.7332 | 2.208 | 0.475 | 2.334 | 252.761m | 4.112m |

The circuits (a), (b), (c) are identical to 2.2 of handwrite handwork 2. We can use the same calculation methods employed in the handwrite homework to acquire the Vout, max & Vout, min.

The maximum output swing is defined as the difference between the maximum and minimum output voltages. This is limited by the bias voltage Vout, bias caused by setting Vicm to 1V. The output swing is given by the following equation:

Next, to determine the max amplitude of the input signal, I use the following equation:

= *Max Input Amplitude*

This helps us find a suitable input that satisfies the requirement of the problem and keeps all transistors in saturation.

**Circuit (a) Waveform & MOSFET Operating Region:**

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自動產生的描述

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自動產生的描述

**Circuit (b) Waveform & MOSFET Operating Region:**

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自動產生的描述

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自動產生的描述

**Circuit (c) Waveform & MOSFET Operating Region:**

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自動產生的描述

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自動產生的描述

**Code for Problem 2 & 3:**

1. \*\*\*-----------------------\*\*\*

2. \*\*\*        setting        \*\*\*

3. \*\*\*-----------------------\*\*\*

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5. .TEMP 25

6. .op

7. \*\*\*-----------------------\*\*\*

8. \*\*\*       simulation      \*\*\*

9. \*\*\*-----------------------\*\*\*

10. .option post

11. .tran 0.1n 30u

12. .probe I(M1\_n)

13. .probe I(M2\_n)

14. .probe Vout=V(x,y)

15. \*.DC Vgs  0V 1.8V 0.05V sweep T 0 80 10

16.

17. \*\*\*-----------------------\*\*\*

18. \*\*\*      parameters       \*\*\*

19. \*\*\*-----------------------\*\*\*

20. .global VDD GND Vbs Vb

21. \*\*\*-----------------------\*\*\*

22. \*\*\*      power/input      \*\*\*

23. \*\*\*-----------------------\*\*\*

24. Vsupply VDD GND 3v

25. \*              SIN(Offset   Amplitude   Freq.   Delay )

26. V1      Vbs GND 0.6v

27. V2      Vb  GND 2v

28. Vcm     N0  GND 1v

29. V4      Vdiff  GND SIN(0   1m   100k  0)

30. EV+     V\_diff+ N0 Vdiff GND +0.5

31. EV-     V\_diff- N0 Vdiff GND -0.5

32. \*\*\*-----------------------\*\*\*

33. \*\*\*        circuit        \*\*\*

34. \*\*\*-----------------------\*\*\*

35. R1  VDD  X   5k

36. R2  VDD  Y   5k

37. M1\_n  X  V\_diff+    Virtual       GND    n\_18\_mm w=45u l=0.3u

38. M2\_n  Y  V\_diff-    Virtual       GND    n\_18\_mm w=45u l=0.3u

39. M5\_n  Virtual  Vbs        GND     GND    n\_18\_mm w=75u l=1u

40.

41. .subckt CKT\_A   Vin\_pos Vin\_neg  X   Y

42. R1  VDD  X   5k

43. R2  VDD  Y   5k

44. M1\_n  X  Vin\_pos    V       GND    n\_18\_mm w=45u l=0.3u

45. M2\_n  Y  Vin\_neg    V       GND    n\_18\_mm w=45u l=0.3u

46. M5\_n  V  Vbs        GND     GND    n\_18\_mm w=75u l=1u

47. .ends

48.

49. .subckt CKT\_B   Vin\_pos Vin\_neg  X   Y

50. M3\_p  X  X          VDD     VDD    p\_18\_mm w=10u l=0.3u

51. M4\_p  Y  Y          VDD     VDD    p\_18\_mm w=10u l=0.3u

52. M1\_n  X  Vin\_pos    V       GND    n\_18\_mm w=45u l=0.3u

53. M2\_n  Y  Vin\_neg    V       GND    n\_18\_mm w=45u l=0.3u

54. M5\_n  V  Vbs        GND     GND    n\_18\_mm w=75u l=1u

55. .ends

56.

57. .subckt CKT\_C   Vin\_pos Vin\_neg  X   Y

58. M3\_p  X  Vb         VDD     VDD    p\_18\_mm w=10u l=0.3u

59. M4\_p  Y  Vb         VDD     VDD    p\_18\_mm w=10u l=0.3u

60. M1\_n  X  Vin\_pos    V       GND    n\_18\_mm w=45u l=0.3u

61. M2\_n  Y  Vin\_neg    V       GND    n\_18\_mm w=45u l=0.3u

62. M5\_n  V  Vbs        GND     GND    n\_18\_mm w=75u l=1u

63. .ends

64.

65. .end

**Problem 3:**

|  |  |  |  |
| --- | --- | --- | --- |
|  | DC Gain (V/V) | Rout (Ω) | Output Swing(V) |
| (b) | -4.0028 | 2.0583k | 1.33184 |
| (c) | -30.7332 | 15.7615k | 3.71792 |

(b) is a differential amplifier biased using diode-connected transistors M3 & M4, while (c) is biased using PMOS current sources. The diode-connected transistors provide a **fixed voltage drop** and are easier to implement, but they don't provide optimal performance in terms of output swing or gain. he diode connection reduces the voltage swing at the output because part of the supply voltage is consumed by the voltage drop across M3​ and M4​. The current-source biasing provides **higher output swing** and **better gain** compared to diode-connected biasing. It also allows more flexibility in controlling the current flowing through the differential pair by adjusting Vb.

|  |  |  |
| --- | --- | --- |
|  | Diode-Connected | Current Source |
| Pros | Simple to Implement | Higher Gain, Larger Output Swing |
| Cons | Sacrifices Gain, Output Swing & Input CM Range | More Complex to Implement |